IN THE SPECIFICATION:

Please amend the specification as follows:

[0001] The present invention relates to a read-only memory (ROM) and the fabrication thereof. More particularly, the present invention relates to an ultraviolet-programmable ~~UV-programmed~~ P-type mask read-only memory (Mask ROM) and ~~the~~ a fabrication thereof.

[0004] However, some problems are encountered in the modified process described above when the dosage of the blanket erasing implantation is poorly controlled. Specifically, when the dosage of the blanket erasing implantation is insufficient, the leakage problem still remains. When the dosage is too high, however, plenty of dopants will diffuse laterally into the channel to cause the Short Channel Effect (SCE).

[0005] Accordingly, this invention provides an ultraviolet-programmable ~~UV-programmed~~ P-type Mask ROM and a method for fabricating the same to prevent a leakage between the bit lines.

[0006] This invention provides a method for fabricating an ultraviolet-programmable ~~UV-programmed~~ P-type Mask ROM without a blanket erasing implantation. Therefore, the method can prevent the leakage problem or the short channel effect caused by an insufficient dosage or an excess dosage of the blanket erasing implantation in the modified P-type Mask ROM process in the prior art.

[0007] The method for fabricating an ultraviolet-programmable ~~UV-programmed~~ P-type Mask ROM of this invention is described below. At first, all memory cells are formed having raised threshold voltages to be in a first logic state ("0" or "1"), in which the channel is hard to switch on. This can be done by, for example, forming a heavily doped N-well for the memory cells. A charge trapping layer is formed on the substrate comprising, for example, a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer. Subsequently, a plurality of bit lines ~~are~~ is formed in the heavily doped N-well and then an insulating layer, such as a thermal oxide layer, is formed on the bit lines. A conductive layer is formed on the substrate and then patterned into a plurality of word lines, wherein the substrate under a word line and between two bit lines serves as a memory cell. The patterning step is conducted by using the bottom oxide layer of the ONO layer as an etching termination layer, for example. An UV-blocking layer, such as an UV-absorbable layer, is formed over the substrate and then a plurality of openings ~~are~~ is formed in the UV-blocking layer to expose selected memory cells that are predetermined to be in a second logic state ("1" or "0"). An UV light is used to irradiate the substrate to inject electrons into the charge trapping layer under the openings to complete the programming process.

[0008] The ultraviolet-programmable ~~UV-programmed~~ P-type Mask ROM of this invention comprises a heavily doped N-well in a substrate, a plurality of bit lines in the heavily doped N-well, a plurality of word lines crossing over the bit lines, a charge trapping layer between the heavily doped N-well and the word lines, and an UV-blocking layer over the substrate. The UV-blocking layer is, for example, an UV-absorbable layer and has a plurality of openings over selected memory cells therein, and the selected memory cells are written by using UV light. The memory cells covered by the UV-blocking layer are in a first logic state ("0" or "1") and the UV-written memory cells are in a second logic state ("1" or "0").

[0012] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. ~~In the drawings,~~

[0013] FIG. 1A~6A and FIG. 1B~6B illustrate a process flow of fabricating an ultraviolet-programmable ~~UV-programmed~~ P-type Mask ROM according to a preferred embodiment of this invention in a cross-sectional view and in a top view, respectively.

[0014] Refer to FIG. 1A~6A and FIG. 1B~6B, which illustrate a process flow of fabricating an ultraviolet-programmable ~~UV-programmed~~ P-type Mask ROM according to the preferred embodiment of this invention in a cross-sectional view and in a top view, respectively.

[0017] Refer to FIG. 3A and 3B, a plurality of word lines 114 ~~are~~ is formed on the substrate 10 with the following steps, for example. A conductive layer (not shown) like a polysilicon layer is formed on the substrate 10. The conductive layer is then patterned to form the word lines 114 perpendicularly crossing over the bit line 110, wherein the bottom oxide layer 104 of the charge trapping layer 102 serves as an etching termination layer. Thus the nitride layer 106 exists under the word lines 114 only.

[0018] Refer to FIG. 4A and 4B, an UV-absorbable layer 112 is formed over the substrate 10. The formation of the UV-absorbable layer 112 can be integrated into a contact process of the periphery circuit and therefore comprises a protective layer 116, an anti-reflection coating (ARC) 118 and an inter-layer dielectric layer (ILD) 120. The anti-reflection coating 118 is formed by, for example, chemical vapor deposition (CVD).

[0019] Refer to FIG. 5A and 5B, a plurality of openings 124 ~~are~~ is formed in the UV-absorbable layer 122 over selected memory cells 128a, which are predetermined to store e-bit "1". An UV light 126 is used to irradiate the substrate 10 to inject electrons into the ONO charge trapping layer 102 of the selected memory cells 128a under the openings 124 for programming. The selected memory cells 128a written with UV light are in a state "1", while the other memory cells 128b are still in the state "0". Since electrons can be trapped only in the nitride layer 106 and the nitride layer 106 outside the word line 144 is removed, the electrons can be confined in the charge trapping layer 102 under the word lines 114 not covered by the openings 124. Therefore, the threshold voltages of the written memory cells 128a can be lowered specifically.